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REMARKS

This case has been carefully reviewed and analyzed in view of the Official Action dated 14 February 2002. Responsive to the rejections made in the Official Action, Claims 1-8 have been canceled by this Amendment and new Claims 9-19 have been inserted for further prosecution in this case.

In the Official Action, the Examiner objected to the entire disclosure as being replete with errors in form, grammar, spelling, and punctuation. Accordingly, the following changes to the disclosure are submitted herewith:

1. A supplemental copy of the original Application papers are enclosed herewith as per the Examiner's request. The supplemental Application papers are as originally filed, except that the lines of text are double-spaced, the text is printed on good quality paper, non-printable characters have been removed and non-English characters have been removed. The substantive content of the new Application papers is exactly that of the original Application, as filed.
2. The Title of the Invention, as originally filed, has been replaced with a brief but technically accurate and descriptive Title, "DIGITAL FM DEMODULATOR WITH REDUCED QUANTIZATION NOISE".
3. The Abstract, as originally filed, has been deleted in its entirety and

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replaced by a Substitute Abstract to correct the numerous errors contained therein. It is believed that the Substitute Abstract now possesses proper form.

4. The Specification has been amended by replacement of the original Specification, as filed, with the Substitute Specification, which was the most efficient means to correct the numerous idiomatic, grammatical, and translational errors found therein. It is believed that the subject matter disclosed by the Substitute Specification was previously disclosed in the Specification and Claims, as filed, and the accompanying Drawing Figures. No new matter has been added by these changes. Additionally, a marked-up copy of the Supplemental Specification described above is attached to this Amendment in compliance with MPEP § 608.01(q). The Substitute Specification includes the same changes as are indicated in the marked-up copy of the Supplemental Specification.

In the Official Action, the Examiner rejected Claims 1, 2, and 4-8 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The Examiner found the Claims to be generally narrative and indefinite and containing numerous grammatical and idiomatic errors. As previously indicated, the original Claims, as filed, have been canceled by this Amendment and new Claims 9-19 have been

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inserted for further prosecution in this case. It is believed that the new Claims clearly and unambiguously define the metes and bounds of the instant invention, for which Patent protection is being sought.

The Examiner rejected Claims 1-8 under 35 U.S.C. § 102(b) as being anticipated by Hunsinger, et al. (U.S. Patent #5,465,396; hereinafter Hunsinger). The Examiner found that the reference discloses the method of operation of the invention of the subject Patent Application, as originally claimed.

Before discussing the prior art reference relied upon by the Examiner, it is believed beneficial to first briefly review the structure of the invention of the subject Patent Application. The invention of the subject Patent Application is a digital FM demodulator used in radio communication systems such as pagers, cellular phones, Global Positioning Satellite (GPS) systems, and Digital Enhanced Cordless Telecommunication (DECT) systems. The system utilizes a phase compensating feedback loop similar to that found in phase locked loops (PLL). The system also has elements and structure in common with Delta-Sigma analog-to-digital (A/D) converters to reduce quantization errors in producing the digital output sequence from a continuously-variable phase-proportional voltage level. The elimination of quantization error is especially imperative in the demodulation or decoding of digital signals in that the quantized error does not effect the output signal's

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amplitude, but rather places erroneous bit patterns into the digital time sequence. That is to say, that a slight quantization error can cause a received bit to be in a logical "1" state when that bit was originally transmitted in a logical "0" state.

A modulated signal  $A_i$  containing digitally encoded information on an intermediate frequency (IF) signal is presented to the input of a segmented reference delay line which includes a course delay line for introducing a fixed delay into the input signal, and a fine delay line which is used to introduce a variable delay in discrete levels to the input signal. The fine delay line has coupled thereto a series of output taps, each of which are connected at the output of each of a series of discrete delay elements. The signal at each of the output taps is a delayed copy of the input signal, the delay time of each being the sum of the delay time of the course delay line and the sum of the delay times of each fine delay element through which the output signal has passed up to the subject output tap.

The output taps of the fine delay line are coupled to respective inputs of an M-to-1 multiplexer. The multiplexer selectively couples one of the input terminals thereof to the output terminal thereof such that the signal at the output of the multiplexer is a selected one,  $A_{id}$ , of the delayed copies of the input signal taken from the fine delay line.

Delayed signal  $A_{id}$  and input signal  $A_i$  are coupled to the input of a phase detector.

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The phase detector produces an output pulse at its output port proportional in width to the phase difference between  $A_i$  and  $A_{id}$ . The output pulses of the phase detector are signed; they convey, by being either positive or negative, whether the signal  $A_{id}$  leads or lags the signal  $A_i$ .

The output port of the phase detector is coupled to a charge pump circuit, or charge integrator. The charge integrator produces a signal at its output proportional to an amount of stored charge accumulated therein. The storage of charge is controlled through the output pulses, received over time, from the phase detector. When the output pulse of the phase detector is positive, i.e.,  $A_{id}$  leads  $A_i$ , charge is added to the charge accumulator and when the output pulse of the phase detector is negative, i.e.,  $A_i$  leads  $A_{id}$ , charge is removed from the charge integrator. The output of the charge pump,  $V_f$ , increases and decreases according to the relative phase between  $A_i$  and  $A_{id}$ .

The output of the charge pump circuit is coupled to the input of a quantizer for producing the final digital output signal at the quantizer output terminal. Typically, the quantizer is an A/D converter. In the Delta-Sigma A/D converter configuration, as utilized by the subject digital FM demodulator, the quantizer is a 1-bit A/D converter or a voltage comparator. The quantizer converts  $V_f$  into a digital output sequence,  $y$ , by forcing a change in state of the output signal when  $V_f$  crosses a reference voltage level.

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A feedback mechanism is implemented through a digital integrator which takes at its input the digital output sequence  $y$  and produces at its output a binary delay selection word. The digital integrator may be a digital up/down counter which counts up when the state of output signal  $y$  is a logical "1", and counts down when the output signal  $y$  is a logical "0". The delay selection word at the output of the digital integrator is presented to the selection port of the multiplexer to select one of the delayed input signals to present to the phase detector circuit at the next cycle or sampling period.

One advantage of the subject digital FM demodulator is that it requires no external clock for a timing reference. The components of the demodulator are synchronized through the modulated signal  $A_i$ . The output pulses of the phase detector are defined by the rising edge of  $A_i$  and the rising edge of  $A_{id}$ . The charge in the charge integrator is output as  $V_f$  before the falling edge of  $A_i$ . The falling edge of  $A_i$  is optionally used to trigger the quantizer and counter. This timing and its relationship to the frequency of the digital output signal of the system realizes an inherent low pass digital filter in the demodulator system. It is the inherent low pass filter that reduces the quantization noise introduced by the quantizing process when producing the digital output sequence.

As stated hereinabove, the Examiner rejected Claims 1-8 under 35 U.S.C. § 102(b) as being anticipated by Hunsinger. Although the invention of Hunsinger is shown as

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having several elements in common with the subject digital FM modulator, important differences exist due to the nature of the output signal produced by each system.

Hunsinger does not seek to extract a digital sequence and does not, therefore, recognize the problems associated therewith. Hunsinger's invention produces at its output an analog signal, i.e., one having a continuously variable amplitude which, if quantization error were to occur therein, only a minute deviation from an optimal amplitude would occur. In systems relying on analog signals for the conveyance of information, such errors in the reconstructed amplitude of a signal are unlikely to produce a catastrophic degradation in the information being transmitted. In the production of digital sequences, quantization errors result in incorrect data being inserted into the data stream, i.e., errors occur along the time axis. Errors of this type can render the information being conveyed undecipherable. Thus, the system of the present invention is designed to greatly reduce the occurrence of such errors.

As Hunsinger does not teach a digital demodulator, the reference does not show or suggest the use of a "quantizer configured to produce a digital output signal at an output terminal thereof" as implemented by the present invention, as now claimed. Furthermore, Hunsinger does not show or suggest the feedback structure of the present invention, i.e., "a digital integrator coupled to said digital output signal, wherein said digital integrator is

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coupled to [a] multiplexer for selectively applying a delay". Only through the quantizer of the present invention is a digital output sequence produced and only through the feedback of the digital output sequence to select the appropriate delayed input signal for the next cycle is the inherent digital filter realized to reduce the quantization error of the quantizer. Hunsinger shows a process for controlling the digital delay through the phase detection process, not through feedback from the output signal. Whereas the feedback structure of the instant invention operates to minimize the phase difference detected by the phase detector, much like a PLL, Hunsinger's open-loop design does not.

Hunsinger's objective is in providing the ability to cancel or filter out an undesired signal through a tracking delay element notch filter, which is adjusted continuously in response to the instantaneous frequency of a dominating interference signal (Column 6, Lines 26-58).

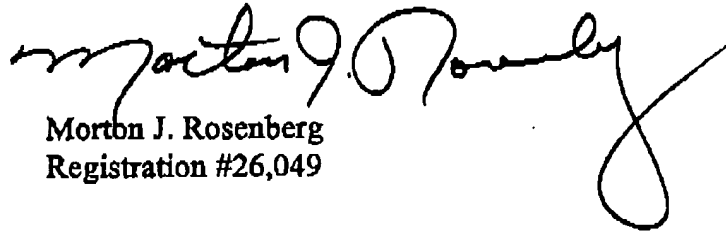
As previously stated, Hunsinger fails to disclose a "quantizer configured to produce a digital output signal at an output terminal thereof", nor "a digital integrator coupled to said digital output signal, wherein said digital integrator is coupled to [a] multiplexer for selectively applying a delay". Therefore, it is respectfully submitted that Hunsinger does not anticipate the invention of the subject Patent Application, as now claimed. Moreover, as Hunsinger does not show or suggest the combined elements for

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the purposes and objectives of producing a digital output sequence in the manner set forth in the subject Patent Application and as discussed hereinabove, it is submitted, respectfully, that the subject digital FM demodulator is not made obvious by the Hunsinger reference, either.

It is now believed that the subject Patent Application has been placed in condition for allowance, and such action is respectfully requested.

Respectfully submitted,

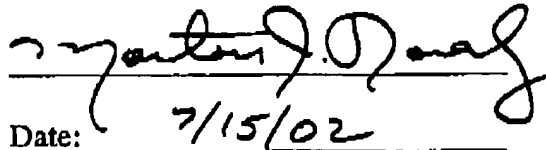


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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this paper is being facsimile transmitted to Art Unit #2631 in the U.S. Patent and Trademark Office on the date shown below.



Date: 7/15/02

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Jieh-Tserng Wu, et al. :  
Serial No: 09/327,178 : Art Unit #2631  
Filed : 7 June 1999 : Examiner:  
Title : METHOD OF DIGITAL FM  
DEMODULATOR :

REQUEST FOR EXTENSION OF TIME UNDER RULE 1.136

Honorable Commissioner for Patents  
Washington, D.C. 20231

Sir:

Applicant hereby requests an Extension of Time for two (2) months to respond to the outstanding Official Action dated 14 February 2002. An Amendment is being filed concurrently with this Request for Extension of Time, which is believed to place the case in condition for allowance.

A check in the amount of \$200.00 is hereby enclosed to cover the filing fees associated with this Extension of Time. If there are any further fees necessary in this filing, the Director of Patents and Trademarks is hereby authorized to charge such to Deposit Account #18-2011.

Respectfully submitted,



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## MARKED-UP SUBSTITUTE ABSTRACT

## ABSTRACT OF THE DISCLOSURE

The present invention relates to a new method of digital FM demodulator that utilizes the delay lines as timing reference and the concept of delta-sigma analog-to-digital conversion to implement the function of time-to-digital conversion. The FM demodulator is constructed from a multiplexer, phase detector, charge pump circuit, quantizer and digital integrator. The modulated signal in intermediate frequency segment passes through the delay lines around one cycle time and is then phase compared with original input modulation signal and the comparison produces a voltage which is compared pulse converted into voltage and stored in a capacitor by way of charge pump circuit. The quantized voltage has been accumulated, then re-select a new delayed output signal to compare its phase with input signal. Meanwhile, the phase difference between input signal and delayed signal is similar to PLL, is a feedback system. This quantized digital signal again pass is used to select a delay for the delayed signal for the next cycle. The phase difference is continuously evaluated through a low-pass filter to filter out high frequency quantized noise to get the original digital modulation signal. and adjusted to produce zero phase difference, much like a phase-locked loop. In this manner, the digital modulation signal is collected at the system output.

# MARKED-UP SUBSTITUTE SPECIFICATION

## ~~A New Method Of Digital FM Demodulator~~

### DIGITAL FM DEMODULATOR WITH REDUCED QUANTIZATION NOISE

#### BACKGROUND OF THE INVENTION

##### *Invention*

##### 1. Field of the ~~invention~~

The present invention relates to a ~~new method of~~ digital frequency-  
(FM) demodulation modulation/demodulator and more particularly, to a digital ~~frequency~~ <sup>FM</sup>  
modulation/demodulator that ~~using the structure of time-to-digital converter and~~  
*extracts a digital time sequence from an intermediate*  
modulation demodulator ~~the concept of delta-sigma analog-to-digital converter~~  
*frequency (IF) carrier while reducing quantization error and eliminating*  
*a requirement of a reference clock.*

##### *of the*

##### 2. Description ~~Of The~~ Prior Art

The Frequency modulation (FM) is ~~one of~~ <sup>an</sup> important and common method <sup>of information conveyance</sup> in  
radio communication system ~~that its~~ <sup>The</sup> receiver end <sup>of the system</sup> contains the FM  
demodulation circuit which ~~often using~~ <sup>is</sup> analog design circuit and the  
conventional analog style FM demodulation circuit including detector circuit and  
a phase lock loop/circuit. <sup>(PLL)</sup> ~~If bring the detector into integrated circuit, then it need~~  
*a larger*  
*is required* bigger chip area ~~and if implement PLL into integrated circuit, then an external~~  
*the* capacitor is necessary outside ~~this chip.~~ <sup>the</sup>

If the modulated signal ~~need the~~ <sup>requires</sup> digital signal <sup>processing</sup> after  
demodulation, then the ~~above two circuit~~ <sup>described above</sup> need analog-to-digital converter to  
convert the demodulated analog signal into digital signal. ~~meanwhile, this~~ <sup>The</sup>  
analog signal is ~~easy to be~~ <sup>easily</sup> interfered by noise signal. ~~However, the digital FM~~  
*To reduce noise*  
demodulator will first convert the ~~modulation~~ <sup>modulated</sup> intermediate-frequency (IF) signal

*Often, the necessary circuitry to implement an FM demodulator*  
*is constructed on an integrated circuit chip.*

into <sup>a</sup>digital signal by way of <sup>an</sup>analog-to-digital converter, <sup>thereafter a</sup>then using <sup>the</sup>digital signal processor to demodulate <sup>the conventional</sup>this modulation signal. The analog-to-digital converter and digital signal processor used in <sup>operate at high</sup>digital FM demodulator must <sup>have fast</sup>have fast speed to demodulate the modulation signal in real time. <sup>The system</sup>It also <sup>could use a</sup>could use a reference clock with <sup>a</sup>multiple-fold frequency of modulation signal for sampling the input ~~modulation~~ <sup>and</sup>signal to detect its phase change <sup>the signal</sup>then demodulate, but such technology <sup>requires</sup>need a high frequency reference clock.

The conventional methods of digital RF communication ~~system~~ always need to convert the analog signal into digital signal in the receiver end with the drawbacks <sup>of</sup>that increasing the circuit complexity. Thus, <sup>a</sup>the demodulation circuit <sup>combining</sup>combines the detector circuit <sup>of a</sup>or PLL with <sup>a carefully chosen</sup>analog-to-digital circuit <sup>to reduce quantization error</sup>could simplify result in accurate demodulation while simplifying circuit design. <sup>the circuit design also will be one of major objectives today.</sup>

## SUMMARY OF THE INVENTION

It is therefore a primary objective of the present invention to provide a new method of digital FM demodulator will be applicable <sup>to</sup>in radio communication system, <sup>such as pagers,</sup>besides, the modulation-demodulation section in receiver end also <sup>Global Positioning Satellite (GPS) system, and (DECT) system</sup>could be applicable in <sup>Digital Enhanced Cordless Telecommunication (DECT)</sup>BB call, cellular phone, <sup>and</sup>GPS system, and <sup>and</sup>DECT system.

The next objective of the present invention is to provide a digital FM <sup>implemented</sup>demodulator <sup>an</sup>with two function of modulation-demodulation and <sup>an</sup>analog-to-digital

converter. The input intermediate-frequency signal <sup>passes</sup> through <sup>the inventive</sup> this invention <sup>thereby generating</sup> a digital signal including <sup>a</sup> high-frequency <sup>quantization noise</sup> quantized signal. Then, by way of a low-pass filter <sup>the</sup> to filter out above <sup>quantized noise signal is filtered</sup> quantized noise signal is filtered. <sup>acquire</sup> <sup>baseband</sup> to get the <sup>baseband</sup> signal.

<sup>A further</sup> The other <sup>adapts a</sup> objective of the present invention is to provide a digital FM demodulator which <sup>adopts the</sup> PLL structure and utilize <sup>conversion does not require</sup> the concept of delta-sigma analog-to-digital <sup>converter</sup> which <sup>without connect</sup> external components <sup>or a</sup> and high frequency reference clock <sup>so that easy for integration</sup>.

The present <sup>provides over similar systems in the prior art by using</sup> this invention with <sup>advantages</sup> that not only use delay lines as the timing <sup>and by adapting</sup> reference <sup>but also adopt the concept of delta-sigma analog-to-digital</sup> <sup>conversion</sup> converter to achieve the time-to-digital conversion <sup>of demodulation</sup> for digital FM <sup>demodulator</sup>. This digital FM demodulator <sup>includes</sup> including delay lines, <sup>m-to-1</sup> multiplexer, <sup>a</sup> phase detector, <sup>a</sup> charge pump circuit, <sup>a</sup> quantizer and <sup>a</sup> digital integrator. The modulation <sup>on an</sup> signal <sup>in</sup> intermediate frequency <sup>carrier</sup> segment <sup>each having a</sup> pass through the delay lines <sup>with the</sup> delay time <sup>of</sup> around one cycle time, and this <sup>the phase of the</sup> delayed signal <sup>is</sup> compared <sup>with the</sup> its phase <sup>of the</sup> with original signal. This <sup>comparison produces a</sup> compared pulse <sup>which is applied to the</sup> will go through charge pump circuit where <sup>a cumulative charge is</sup> a charge <sup>is</sup> into a level which <sup>and convert into a voltage level</sup> stored in capacitor. This <sup>quantized</sup> quantized voltage <sup>is</sup> is accumulated by the digital integrator. Then <sup>a new of</sup> sample <sup>another output signal of the</sup> delay lines <sup>is taken</sup> and compare <sup>d in</sup> phase with <sup>the</sup> input signal. This system is similar to PLL, i.e., <sup>taking phase as the error signal</sup> it is a feedback system. The quantized digital signal will feed through <sup>the</sup> low-pass

defined by the sampling rate of the system

filter to filter out high frequency noise and get the original modulation signal, i.e.,

the modulation signal is a digital signal.

### BRIEF DESCRIPTION OF THE DRAWINGS

The drawings disclose an illustrative embodiment of the present invention, which serves to exemplify the various advantages and objects thereof, and are as follows:

Fig.1 is the circuit block diagram of digital FM demodulator according to the present invention.

Fig.2 is the circuit waveform of digital FM demodulator according to the present invention.

Fig.3 is the system structure of digital FM demodulator according to the present invention.

### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

which illustrates the  
Please refer to Fig. 1, ~~that relates to~~ the circuit block diagram of digital FM demodulator. The ~~modulation~~ <sup>modulation</sup> signal,  $A_i(t)$ , is fed into reference delay lines 11, said reference delay lines 11 including coarse delay line 111 and fine delay line 112. ~~those~~ <sup>The</sup> delay time of delay lines 111 and 112 ~~is~~ <sup>are</sup> controlled separately by other circuits. The fine delay lines 112 ~~has~~ <sup>have</sup> multiple output signals  $A_{i1}(t), A_{i2}(t), A_{i3}(t), \dots, A_{ij}(t)$  which could be expressed as follow:

$A_{ij}(t) = A_i(t - T_c - j \cdot \tau)$  ~~(t)~~  
→ Where, <sup>the</sup>  
 $T_c$  the total fixed delay time of coarse delay lines, and  
 $\tau$  the unit delay time of fine delay lines.

<sup>13</sup>  
The phase detector compares the phase difference between  $A_{id}$  and  $A_i$ , then generate up and down signal. The m-to-1 multiplexer will select one of output signal  $A_{i0}(t), A_{i1}(t), A_{i2}(t), \dots, A_{ij}(t)$  from fine delay lines 112 and name it as  $A_{id}$  <sup>the delayed signal</sup>.

signal. If the rising edge of  $A_{id}$  signal lead the  $A_i$  signal, <sup>the</sup> up signal will generate an effective pulse <sup>having a</sup> and its pulse width <sup>equivalent to</sup> is just same as the time difference between the rising edges of  $A_i$  and  $A_{id}$ , <sup>and then</sup> down signal <sup>will not be generated</sup> do not generate any effective pulse. <sup>impressed on the bypassing, the</sup> The total delay time of  $A_i$  signal pass through delay lines is  $T_c + d \cdot \tau$ , <sup>where d is the number of fine delay lines and</sup> and the pulse width will equal to  $T - T_c - d \cdot \tau$  <sup>where "T" is smaller than period T of  $A_i$  signal</sup>.

<sup>similarly</sup>  
In the same way, if the rising edge of  $A_{id}$  signal lag the  $A_i$  signal, <sup>a</sup> down signal will generate an effective pulse <sup>having</sup> and its pulse width <sup>equal to</sup> is also just same as the time difference of  $A_{id}$  and  $A_i$  signal, <sup>i.e.,</sup> and the pulse width will equal to  $T_c + d \cdot \tau - T$ .

The phase detector output

Its value is positive when  $A_{id}$  lead the  $A_i$  signal, while its value is considered negative when  $A_{id}$  lag  $A_i$  signal. Both effective pulse of up and down signal will trigger the charge pump circuit 14 for charging and discharging to capacitor,  $C_c$ , which will generate a voltage difference,  $V_f$ , and its voltage level is proportional to the time difference or phase difference of  $A_{id}$  and  $A_i$  signal.

Each cycle of input modulated signal will generate a  $V_f$  which is accumulated in storage capacitor  $C_c$ , and this stored voltage will be quantized to generate a bit stream digital signal  $y(k)$ , which is the output digital sequence of total system.

Quantizer 15 is an analog-to-digital converter which may be a one-bit or multiple-bit converter. A one-bit converter may be implemented by a voltage comparator. The quantizer 15 is a one-bit voltage comparator. In the preferred embodiment,

Digital integrator 16 accumulates the output digital signal  $y(k)$ , actually, it is simply taking the output of an up-down counter due to quantizer 15 as its input. In the preferred embodiment,

counter output signal will select one output  $A_{id}$  signal from the fine delay lines by way of multiplexer and compare its phase with  $A_i$  signal. Consequently, the delay time of  $A_{id}$  signal is controlled by output signal  $y(k)$ . It will delay one more unit time if  $y(k)=1$ . Conversely, the delay of  $A_{id}$  will decrease one unit delay if  $y(k)=0$ . Thus, this whole system is similar to PLL structure. The output signal  $y(k)$  is fed back to adjust the  $A_{id}$  delay time and make the next rising edge of  $A_i$  signal arrive at phase detector with rising edge of  $A_{id}$  signal simultaneously. So the  $A_{id}$  signal is just delayed one cycle than  $A_i$  signal when the system is locked.

Referring to ~~As shown in Fig. 2, this is~~ the circuit waveforms of digital FM demodulator ~~the~~ according to the present invention. ~~As shown~~ ~~T(k)~~ is the kth cycle time of ~~the modified~~ input modulation signal and ~~P(k)~~ is the time difference of ~~the rising edge of and the~~ rising edge with next ~~Ai~~ cycle. The effective pulse of ~~the~~ up signal means ~~P(k)~~ is ~~a~~ positive value, ~~but~~ the down signal make ~~P(k)~~ negative. ~~That is~~ Because the maximum frequency shift of input modulation signal is much smaller than carrier frequency, ~~the~~ the change of ~~T(k)~~ is small relative to carrier cycle ~~Tc~~.

Therefore, the effective pulse of ~~the~~ up signal and ~~the~~ down signal only happen at the rising edge of ~~Aid~~ and ~~Ai~~ signal ~~the~~ and this effective pulse has been transferred to ~~Vf~~ that is stored in ~~storage~~ capacitor ~~Cc~~ by way of charge pump circuit before ~~the arrival of the~~ falling edge. ~~This~~ The falling edge of ~~Ai~~ used as the trigger clock of the quantizer and counter.

Thus, the system does not require an external reference clock. ~~As shown in~~ That means this system does not need external reference clock. ~~As shown in~~ Fig. 2 waveform diagram, a formula as follows:

$$P(k+1) = P(k) + T(k) - T(k-1) + y(k) \cdot T_c \quad (2)$$

Definition where

$$\Delta T(k) = T(k) - T(k-1) \quad (3)$$

Therefore, we could get

$$P(k+1) = P(k) + \Delta T(k) + y(k) \cdot T_c \quad (4)$$

If ~~V(k)~~ means the capacitor voltage at kth cycle ~~as shown in~~ based on Fig. 2, we could see ~~V(k)~~ signal is generated by ~~V(k-1)~~ and ~~Ic~~ signal to charge/discharge ~~Cc~~

during up or down signal effective pulse period and <sup>an</sup> <sup>to</sup>  $I_b$  charge/discharge  $C_c$  during kth cycle, i.e., the voltage is determined by <sup>these</sup> ~~these~~ three parameters.  $\leftarrow$

<sup>change in</sup> The voltage on  $C_c$  for  $I_c$  at kth cycle is :

$$\Delta V_{f\_a} = I_c / C_c * P(k) \quad \text{--- (5) ---}$$

If the trigger clock is the input modulation signal  $A_i$ , then the  $C_c$  voltage level <sup>change in the</sup> will be next formula when charge-discharge is at kth cycle <sup>the</sup> ~~will be~~

$$\Delta V_{f\_b} = y(k) * I_b / C_c * [T(k) + T(k+1)] / 2 \quad \text{--- (6) ---}$$

Then,

$$\Delta V_f = \Delta V_{f\_a} + \Delta V_{f\_b} \quad \text{--- (7) ---}$$

$$V(k+1) = V(k) + \{y(k) * (I_b / C_c) * [T(k) + T(k+1)] / 2\} + \{I_c / C_c * P(k)\} \quad \text{--- (8) ---}$$

Because the maximum frequency shift is much smaller than carrier frequency, the  $T(k)$  is <sup>approximately</sup> ~~around~~ equal to carrier cycle  $T_c$  and

$$V(k+1) = V(k) + I_c / C_c * P(k) + y(k) * (I_b / C_c) * T_c \quad \text{--- (9) ---}$$

Assume

$$A = I_c / C_c \quad \text{and}$$

$$B = (I_b / C_c) * T_c. \quad \text{Then}$$

We could get next formula

$$V(k+1) = V(k) + A * P(k+1) + B * y(k).$$

<sup>Inserting</sup> Put the  $P(k+1)$  into <sup>the</sup> above formula, <sup>we</sup> ~~then~~ get

$$V(k+1) = V(k) + A * [P(k) + \Delta T(k) + y(k) * T] + B * y(k)$$

The quantized output of  $V(k)$  is the total system output.

Referring to

As shown in Fig. 3, is the system structure of digital FM demodulator

according to the present invention. This diagram is a two level delta-sigma structure. Its input is  $\Delta T(k)$ , that also is the signal difference of  $T(k)$  and  $T(k-1)$ .

The concept of the output signal,  $y(k)$ , of the present invention is similar to a conventional analog-digital converter output signal. In both systems, the quantized noise signal is shifted into the high frequency segment. However, in conventional systems, the output digital signal  $y(k)$  is

first accumulated and then filtered out quantized noise by the digital filter to get the modulation signal.

This technology is similar to conventional delta-sigma analog-to-digital converter. As shown above, Based on above deduction, the output digital signal is the produced by the differentiation of original modulation signal. In brief,  $y(k)$  signal is filtered out the quantized noise by way of low-pass digital filter before signal accumulation.

The present

This invention provides a FM digital demodulator which with more advantages than conventional technology as follow:

1. The method and circuit <sup>of the present invention</sup> will be applicable in radio communication system <sup>such as pager</sup> besides, the modulation-demodulation section in receiver end also could be applicable in BB call, cellular phone, GPS system, and DECT system.
2. The present invention <sup>to</sup> provide a digital modulation demodulator which <sup>adapts a</sup> ~~adopt the~~ PLL structure and utilize the concept of delta-sigma analog-to-digital converter <sup>requiring</sup> without ~~connect~~ external component <sup>or a</sup> and high frequency reference clock <sup>as to allow ease of</sup> so <sup>that easy for</sup> integration.
3. The present invention <sup>to</sup> provide a digital modulation demodulator with ~~two~~ the function of demodulation and analog-to-digital conversion. The input of intermediate-frequency signal pass through <sup>the inventive</sup> this invention demodulator will <sup>and</sup> generate a digital signal including high-frequency <sup>quantization noise</sup> quantized signal. Then, by way of <sup>an inherent</sup> low-pass filter, <sup>the</sup> to filter out above <sup>is altered</sup> quantized noise signal <sup>to get</sup> the <sup>baseband</sup> ~~baseband~~ signal. <sup>acquire</sup>

Many changes and modifications in the above described embodiment of the invention can, of course, be carried out without departing from the scope thereof. Accordingly, to promote the progress in science and the useful arts, the invention is disclosed and is intended to be limited only by the scope of the appended claims.